REMARKS

Claims 8, 10 and 12, have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **March 25, 2004**.

Claim Rejections under 35 USC §112

Claims 7-19 are rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement.

In the Office Action the Examiner provides reasons for rejecting independent claims 7, 14, 16 and 17. However, no reason is provided for the rejection of independent claims 9 and 15. It is the applicant's opinion that claims 9 and 15 should have not been rejected with claims 7, 14, 16 and 17. Therefore, claims 7, 14, and 16-19 have been canceled. With the cancellation of these claims the applicant requests the withdrawal of the rejection of Claims 7-19 under 35 USC §112, first paragraph.

Claims 16 and 17 are further rejected under 35 USC §112, first paragraph, as failing to comply with the written description requirement.

Claims 16 and 17 have been canceled. Therefore, withdrawal of the rejection of Claims 16 and 17 under 35 USC §112, first paragraph, is respectfully requested.

Claim Rejections under 35 USC §102

Claims 7-17 are rejected under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent 6,417,575 B2).

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to 2 x W2 + n x W3 as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3 corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11).

It is a feature of the present invention that the recess is formed so that the insulating regions (21a) are not disposed in a near wiring area (27b) superposed upon an extended area of the wiring part (25) into the pad part (27), within a first frame area (27a).

The Examiner seems to think that the pad part corresponds to the lower wide portion of pad (240) shown in FIG. 77B of Harada, and the wiring part corresponds to a part in a layer (230d) extending toward the left side from the pad (240) shown in FIG.77B or a part extending toward the left side from the pad (240) shown in FIG.77A.

In the present invention, both of the pad part and the wiring part are parts of the recess reaching the bottom of the first intra-layer insulating film. In contrast, the lower wide portion of pad (240) reaches the bottom of the layer (230). However, the part extending toward the left side from the pad (240) shown in FIG.77B of Harada does not reach the bottom of the layer (230). Furthermore, the part extending toward the left side from the pad (240) shown in FIG.77A of Harada is placed in the layer (15d) shown in FIG.77B, but is not placed in the layer (230).

Further, the Examiner seems to think that a plurality of insulating regions correspond to the insulating partition (341) shown in FIGS.77A and 77B of Harada. In FIG.77B, the insulating partition (341) looks like **a *plurality of*** protruding sections. However, as shown in FIG.77A, the metal layer (340) is separated from the lower protruding section (240) by the insulating partition (341). Namely, the insulating partition (341) surrounds the lower protruding section (240). The insulating partition (341) cannot be ***a plurality of*** protruding sections.

In the present invention, the plurality of insulating regions are disposed on the bottom of the pad part of the recess reaching the bottom of the intra-layer insulating film. The wiring is filled in the wiring part of the recess. Namely, both of the plurality of insulating regions and the wiring is placed in the intra-layer insulating film. In contrast, in FIG.77B of Harada, the part extending to

the left side from the pad (240), which corresponds to the wiring of the present invention according to the Examiner's insistence, and the insulating partition (341), which corresponds to the plurality of insulating regions according to the Examiner's insistence, are placed in the different layers.

Furthermore, as shown in FIG.77Aof Harada, the insulating partition (341) surrounds the lower protruding section (240). This means that insulating partition (341) is disposed in a near wiring area. In contrast, the plurality of insulating regions of the present invention are not disposed in the near wiring area.

Therefore, independent claims 9 and 15 patentably distinguish over the prior art relied upon by reciting, as exemplified by claim 9,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 7-17 under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent 6,417,575 B2) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 8, 10 and 12, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/alw
Atty. Docket No. **020029**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

H:\HOME\GSTEVENS\02\020029\Amend 03-25-04 OA